EliteMT

LP62256E Series

32K X 8 BIT CMOS SRAM

Features

- Single +5V power supply
- Access time: 70 ns (max.)
- Current:
  Very low power version: Operating: 70mA (max.)
  Standby: 25μA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2V (min.)
- Available in 28-pin DIP, SOP and TSOP packages

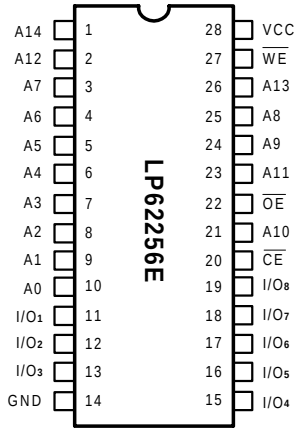
General Description

The LP62256E is a low operating current 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates on a single 5V power supply.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

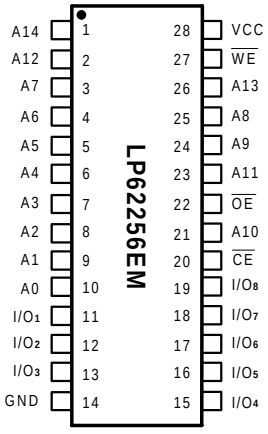
Minimum standby power is drawn by this device when $\overline{CE}$ is at a high level, independent of the other input levels.
Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configurations

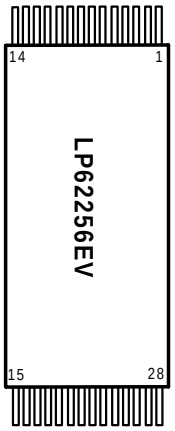
■ **DIP**



■ **SOP**

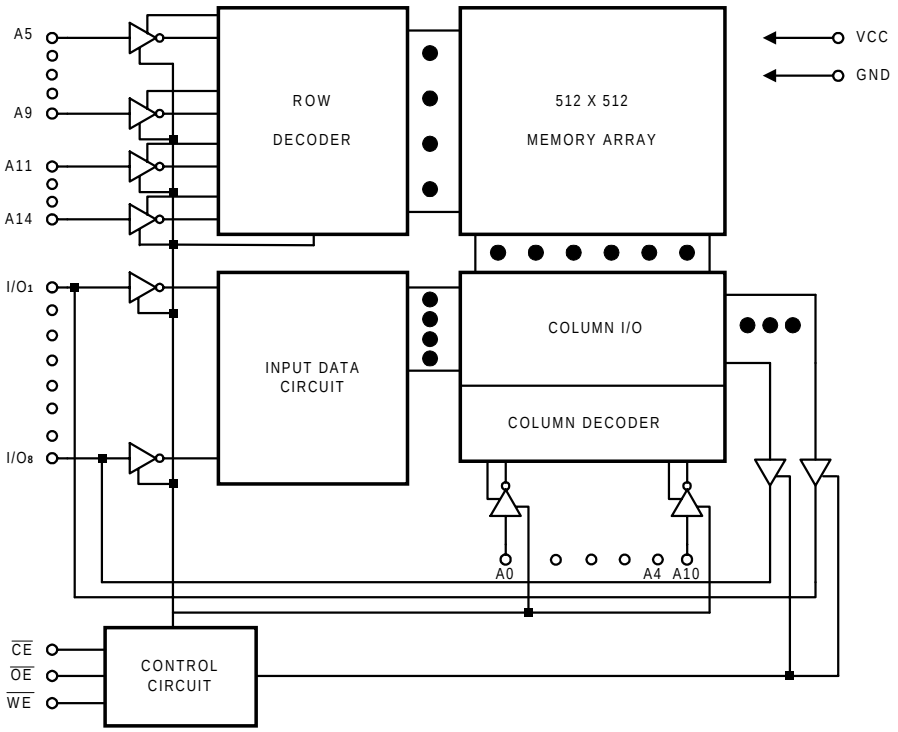


■ **TSOP**



Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Pin Name	$\overline{OE}$	A11	A9	A8	A13	$\overline{WE}$	VCC	A14	A12	A7	A6	A5	A4	A3
Pin No.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
Pin Name	A2	A1	A0	I/O_1	I/O_2	I/O_3	GND	I/O_4	I/O_5	I/O_6	I/O_7	I/O_8	$\overline{CE}$	A10

Block Diagram



Pin Descriptions - DIP/SOP

Pin No.	Symbol	Description
1 - 10, 21, 23 - 26	A0 - A14	Address Inputs
11 - 13, 15 - 19	I/O_1 - I/O_8	Data Input/Outputs
14	GND	Ground
20	$\overline{CE}$	Chip Enable
22	$\overline{OE}$	Output Enable
27	$\overline{WE}$	Write Enable
28	VCC	Power Supply (+5V)

Pin Description - TSOP

Pin No.	Symbol	Description
1	$\overline{OE}$	Output Enable
2 - 5, 8 - 17, 28	A0 - A14	Address Inputs
6	$\overline{WE}$	Write Enable
7	VCC	Power Supply
18 - 20, 22 - 26	I/O_1 - I/O_8	Data Input/Outputs
21	GND	Ground
27	$\overline{CE}$	Chip Enable

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	0	+0.8	V
C_L	Output Load	-	-	100	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to + 7.0V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . 0°C to + 70°C
Storage Temperature, Tstg . . . . . -55°C to + 125°C
Temperature Under Bias, Tbias . . . . . -10°C to + 85°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, VCC = 5V ± 10%, GND = 0V)

Symbol	Parameter	LP62256E-70LL		Unit	Conditions
		Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage Current	-	1	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IH} $V_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	-	15	mA	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{CC1}	Dynamic Operating Current	-	70	mA	Min. Cycle, Duty = 100% $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{CC2}	Dynamic Operating Current	-	15	mA	$\overline{CE}$ = V_{IL}, V_{IH} = VCC V_{IL} = 0V, f = 1MHz $I_{I/O}$ = 0mA

DC Electrical Characteristics (continued)

Symbol	Parameter	LP62256E-70LL		Unit	Conditions
		Min.	Max.		
I_{SB}	Standby Power Supply Current	-	2	mA	$\overline{CE}$ = V_{IH}
I_{SB1}		-	25	µA	$\overline{CE}$ ≥ VCC - 0.2V, V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -1.0mA

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	High Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	L	H	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	X	L	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

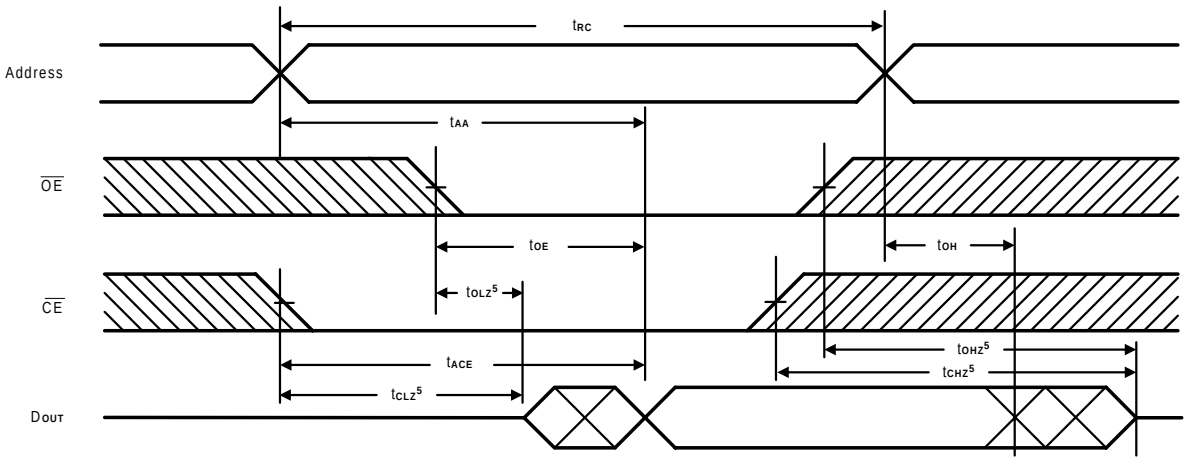
AC Characteristics (T_A = 0°C to + 70°C, VCC = 5V ± 10%)

Symbol	Parameter	LP62256E-70LL		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	70	-	ns
t_{AA}	Address Access Time	-	70	ns
t_{ACE}	Chip Enable Access Time	-	70	ns
t_{OE}	Output Enable to Output Valid	-	35	ns
t_{CLZ}	Chip Enable to Output in Low Z	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	ns
t_{CHZ}	Chip Disable to Output in High Z	0	25	ns
t_{OHZ}	Output Disable to Output in High Z	0	25	ns
t_{OH}	Output Hold from Address Change	5	-	ns
Write Cycle				
t_{WC}	Write Cycle Time	70	-	ns
t_{CW}	Chip Enable to End of Write	60	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AW}	Address Valid to End of Write	60	-	ns
t_{WP}	Write Pulse Width	50	-	ns
t_{WR}	Write Recovery Time	0	-	ns
t_{WHZ}	Write to Output in High Z	0	30	ns
t_{DW}	Data to Write Time Overlap	30	-	ns
t_{DH}	Data Hold from Write Time	0	-	ns
t_{OW}	Output Active from End of Write	5	-	ns

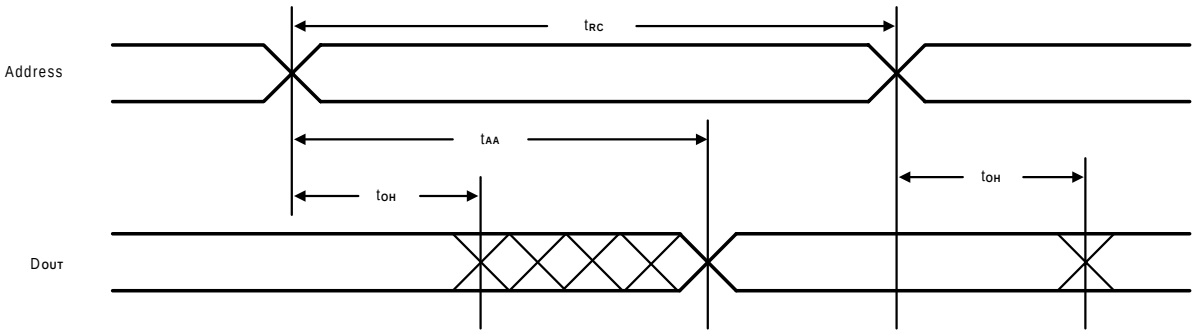
Notes: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

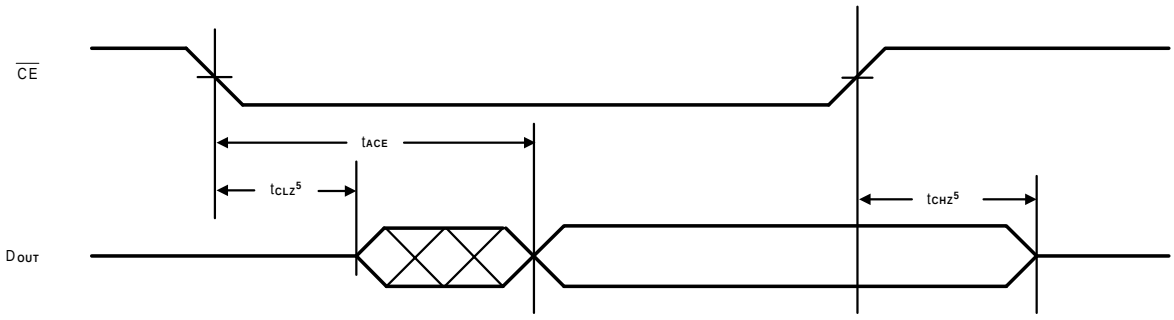
Read Cycle 1 (1)



Read Cycle 2 (1, 2, 4)



Read Cycle 3 (1, 3, 4)

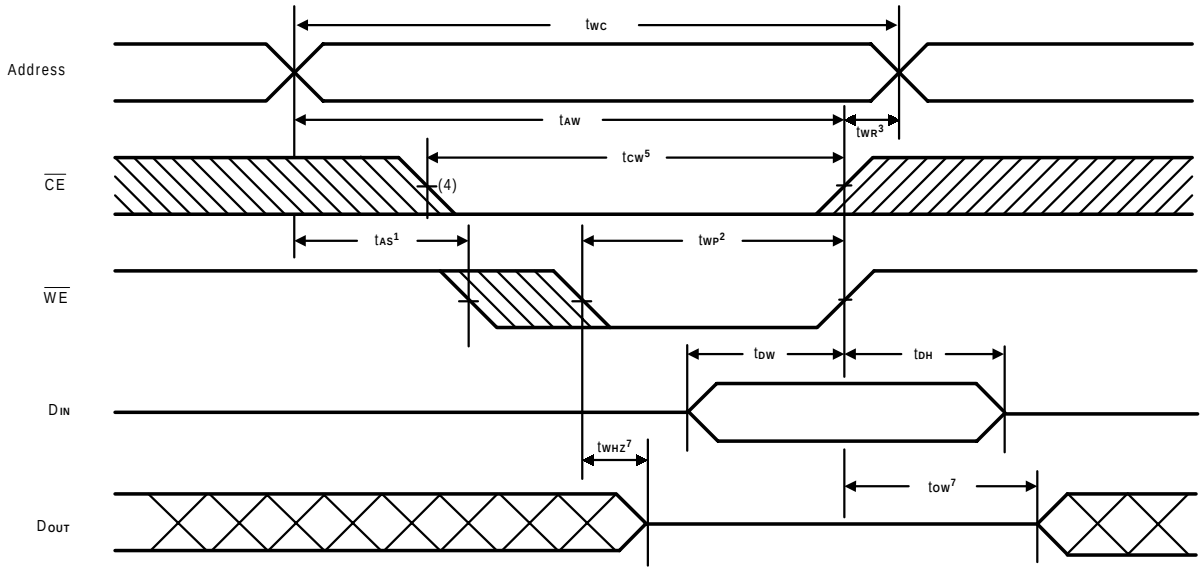


Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Timing Waveforms (continued)

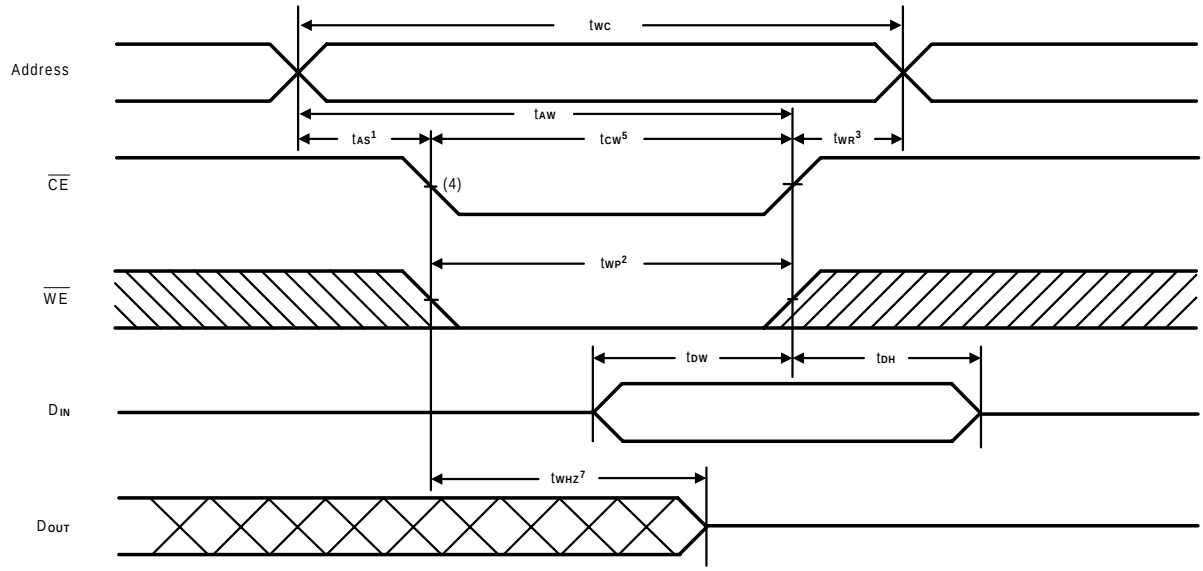
Write Cycle 1[6]

(Write Enable Controlled)



Write Cycle 2

(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.

2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ going high to the end of the Write cycle.
4. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of Write.
6. $\overline{OE}$ level is high or low.
7. Transition is measured ±500mV from steady. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

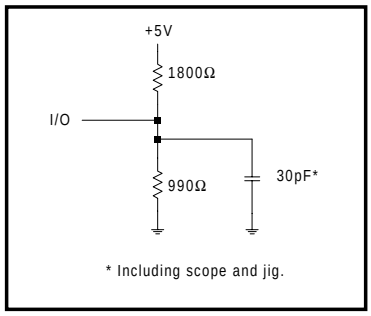


Figure 1. Output Load

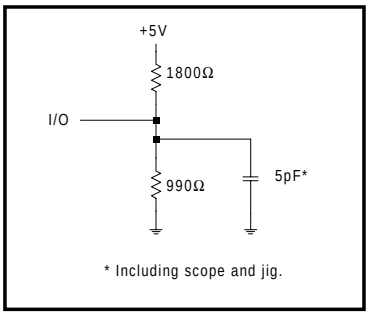


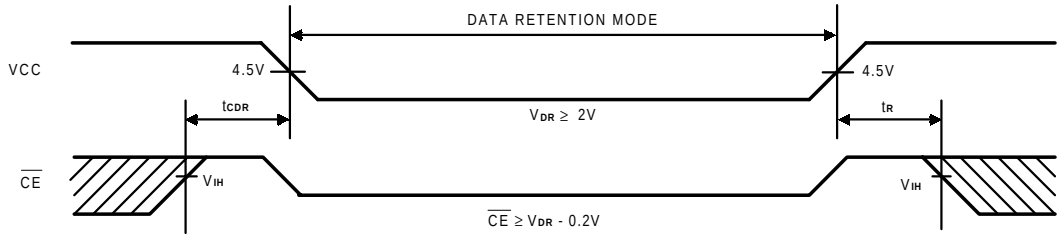
Figure 2. Output Load for t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{CHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention		2.0	5.5	V	$\overline{CE} \geq$ VCC - 0.2V
I_{CCDR}	Data Retention Current	L Version	-	50*	µA	VCC = 3.0V, $\overline{CE} \geq$ VCC - 0.2V, $V_{IN} \geq$ 0V
		LL Version	-	10**		
t_{CDR}	Chip Disable to Data Retention Time		0	-	ns	See Retention Waveform
t_R	Operation Recovery Time		5	-	ms	

** LP62256E-70LL I_{CCDR}: Max. 3µA at T_A = 0°C to + 40 °C

Low VCC Data Retention Waveform

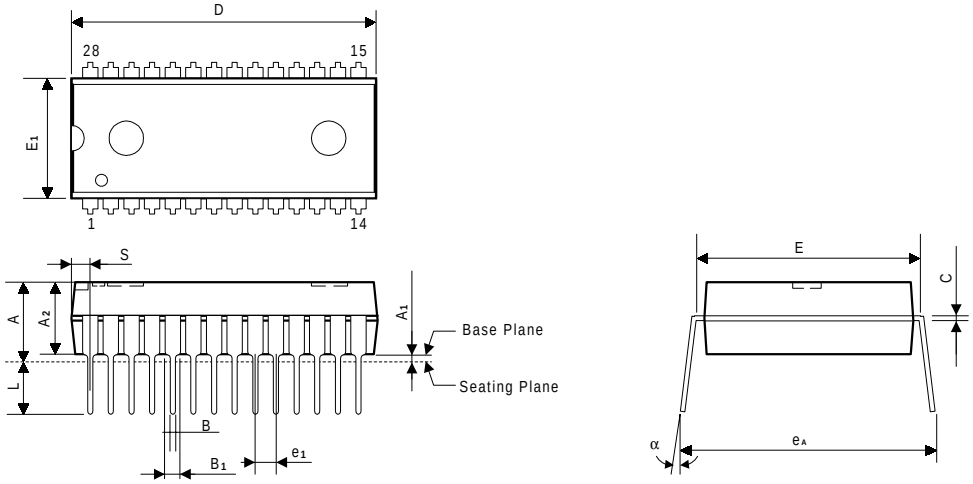


Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (μA)	Package
LP62256E-70LL	70	70	25	28L DIP
LP62256EM-70LL		70	25	28L SOP
LP62256EV-70LL		70	25	28L TSOP

Package Information

P-DIP 28L Outline Dimensions unit: inches/mm

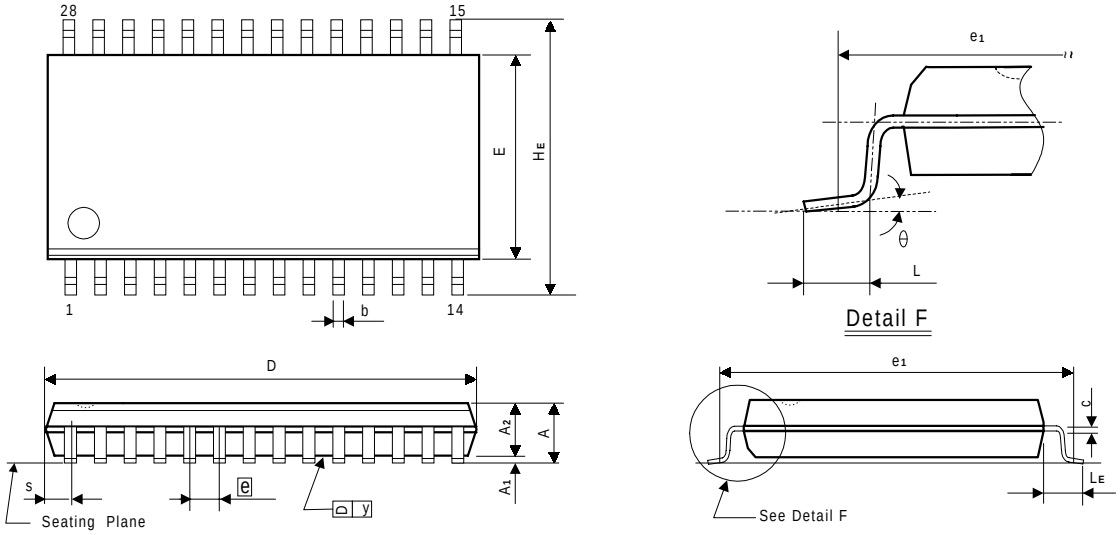


Symbol	Dimensions in inches	Dimensions in mm
A	0.210 Max.	5.33 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.155±0.010	3.94±0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.460 Typ. (1.480 Max.)	37.08 Typ. (37.59 Max.)
E	0.600±0.010	15.24±0.25
E_1	0.550 Typ. (0.562 Max.)	13.97 Typ. (14.27 Max.)
e_1	0.100±0.010	2.54±0.25
L	0.130±0.010	3.30±0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.655±0.035	16.64±0.89
S	0.090 Max.	2.29 Max.

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

Package Information

SOP (W.B.) 28L Outline Dimensions unit: inches/mm

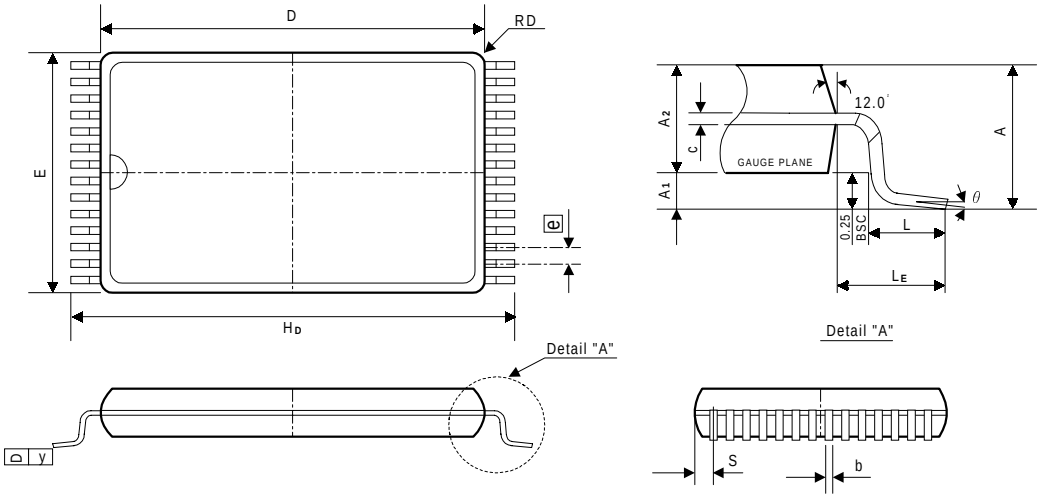


Symbol	Dimensions in inches	Dimensions in mm
A	0.112 Max.	2.85 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.098±0.005	2.49±0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
c	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.713 Typ. (0.733 Max.)	18.11 Typ. (18.62 Max.)
E	0.331±0.010	8.41±0.25
e	0.050 ±0.006	1.27±0.15
e_1	0.429 NOM.	10.90 NOM.
H_E	0.465±0.012	11.81±0.31
L	0.036±0.008	0.91±0.20
L_E	0.067±0.008	1.70±0.20
S	0.047 Max.	1.19 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSOP 28L TYPE I (8 X 13.4mm) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.049 Max.	1.25 Max.
A_1	0.002 Min.	0.05 Min.
A_2	0.039±0.002	1.00±0.05
b	0.0079±0.0012	0.20±0.03
c	0.006±0.0003	0.15±0.008
D	0.465±0.004	11.80±0.10
E	0.315±0.004	8.00±0.10
e	0.0217 TYP.	0.55 TYP.
H_D	0.528±0.008	13.40±0.20
L	0.02±0.008	0.50±0.20
L_E	0.0266 TYP.	0.675 TYP.
S	0.0167 TYP.	0.425 TYP.
y	0.004 Max.	0.10 Max.
θ	0° ~ 6°	0° ~ 6°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.